Prognostics of Electronic Systems through Power Supply Current Trends

Timmy Sundström, Behzad Mesgarzadeh, Mattias Krysander, Markus Klein, Ingemar Söderquist, Anneli Crona, Torbjörn Fransson, Atila Alvandpour

***Abstract*—As today's avionic systems highly rely on electronic components, the prognostic of electronic systems in the context of avionics has become crucial. This paper presents a prognostic method applicable to electronic components and systems based on the analysis of the power supply current. In this method, the focus is on trends in the measured power supply current of the device under prognostic process. The discussion in this paper reveals that there is a measurable relationship between the supply current and the remaining lifetime of the electronic devices. The presented methodology is supported by circuit simulations performed on a system consisting of reference circuitry. The prognostic method shows great promise due to the ability of being applicable at any prognostic level.**

***Index Terms*—Prognostics and Health Management, Electronics, System prognosis, Aging**

I. Introduction

The concept of prognostics is to diagnose and predict remaining useful lifetime (RUL) of a device, component, or system. Future electronic systems with prognostic capability will be able of identifying potential failures in advance and provide information on system health, this information could be used to reduce unscheduled maintenance or to extend service cycles [1], [2]. This prognostic capability offers tremendous advantages since the mean-time-to-restore on an unscheduled maintenance is considerably larger compared to a pre-arranged service occasion [3]. Moreover, the information on impending errors and failures makes it possible to optimize the logistics for replacement of components, i.e. by pre-order of the device that is about to fail. This can limit the spare-part inventory and further reduce the down-time of the system in question.

Today, prognostic concepts and methodologies are developed and implemented for mechanical systems in different complex systems where reliability is the main concern, such as in military and aerospace. Examples on properties to consider in mechanical systems are: vibration, temperature, operation hours, condition of fluids, etc. [4]. These properties are relatively simple to monitor and collect data from. Moreover, the physics and models behind failure precursors for mechanical systems are well known. This provides a solid ground for prognostics and health management (PHM) of mechanical systems.

Electronic systems on the other hand, have traditionally not been subject to prognostic and health management because their time to wear-out has been longer than the life cycle of the whole system [5]. For very deep sub-micron processes this has changed as the circuit life-time for worst-case conditions are down to a few years or even a few months [6], [7].

Life consumption monitoring (LCM) for electronics is different compared to mechanics. There are a number of factors making prognostic and health management for electronic systems more difficult compared to mechanical systems. For instance the complexity, electronic systems have a large number of connected devices each with low probability of failure (often less than 10^{-6} per flight hour). And there are a multitude of failure mechanisms. Detection of deterioration for many of these failure mechanisms is technically possible. However, the sensors might in many cases be more complex and consume larger space (and weight) than the components being monitored [3].

Highly miniaturized electronics and increased reliability was important goals developing electronics for the Gripen Fighter, see Fig. 1. One approach was to minimize the number of solder joint connections at the level of circuit boards and introduce more complex miniaturized modules. Modules containing multiple chips mounted on silicon substrate. The circuit boards used in Gripen have been in operation for 10 years with low failure rate due to connections.

Figure 1. The processor circuit board is part of flight management and tactical mission computer used in the Gripen Fighter.

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With modern aircrafts being increasingly dependent on avionics, the need for robust and accurate prognostic and health management systems will be increasingly important.

This paper will present a study on how measurements of the power supply current of an electronic system could be used to gain information about the health and remaining useful life-time. An advantage with the proposed approach is that the introduction of prognostics to an electronic system does not require any modification of the system, since the power supply current can be measured externally. Furthermore, this approach does not rely on any specific system architecture, making it applicable to a wide range of systems. The concept is introduced by applying the method to two reference systems on the chip level. Based on the nature of the supply current of CMOS circuits the method is scalable to more complex and heterogeneous systems.

This paper is organized as follows: Section II provides a background of the work in the context of avionics. Section III presents the sources of failure for electronic systems in general. Section IV explains the mechanisms behind the dominant on-chip failures and how the aging is modeled for circuit simulations. Section V will show how the measurements of the supply current variations can be used to estimate the health and to prognose the remaining useful life-time of the system. In section VI the method is presented through the simulation of two reference systems. Section VII will discuss the application of the method to more complex systems and how the method is also scalable across the prognostic levels. Finally, Section VIII concludes the presented discussions.

II. Background

A highly developed ability to use aircraft components and systems optimally is advantageous in order to achieve competitiveness on the aircraft market of today. This requires that degradations and impending faults are identified before they cause a failure and that the RUL can be estimated by using prognostic methods. The prognostic ability enables optimal condition-based maintenance and offers the possibility to prolong RUL. Altogether this gives the operator a higher potential of increasing the aircraft uptime and availability.

The ability to predict when an impending fault will have a functional impact also has a positive effect on system safety, maintenance and life cycle costs (LCC). These benefits could be achieved by (1) reducing the need for unscheduled/corrective maintenance actions if faults are detected before they occur, (2) increasing the average useful life of Line Replaceable Units (LRU:s) by estimating the remaining useful life, i.e. by using the units longer than advocated in the maintenance plan if the health condition of the unit permits, (3) preparing for maintenance activities before the aircraft has landed.

This goes well in hand with new contract models for maintenance repair and overhaul that have emerged in the context of Contracting for Availability (CFA): Performance Based Logistics; Integrated Operational Support; Service by the Hour; and Maintenance Free Operating Period. These models enable a fixed-price total solution selling, i.e. the manufacturer not only delivers the technical system and customer support but now also has the end-to-end responsibility for the logistic supply chain [8].

Traditionally prognostics has been concentrated upon expensive mechanical systems such as engines, gear boxes and air frames, for instance crack growth in a turbine engine blade [9] or in a helicopter planetary gear plate [10]. A trend in the aircraft industry is to introduce more electronics into the aircrafts (MEA), exemplified by the Boeing B787 and Joint Strike Fighter JSF which are the first commercial and military aircrafts respectively based upon MEA. The main objective of MEA is to reduce weight, in order to reduce the aircraft fuel consumption. This is realized by replacing mechanical systems by electronics, which in turn has raised demands of using prognostics on electrical components and circuit boards [11]. The following requirement from United States Department of Defense (DoD) illustrates that prognostics is seen as a key enabler for the JSF maintenance system: "The [item] shall incorporate an embedded prognostic capability that will enhance availability and reduce support costs by predicting mission critical failures. Prognostics shall predict at least 70% (with a 95% goal) of the mission critical failures from 480 hours to 96 hours in advance of occurrence with 80% probability" [12].

III. Sources of Failure

As electronic components and systems in avionics tend to inhibit a large amount of failure modes and mechanisms, the understanding of the underlying principles is necessary in the estimation of the current system health. Systems in general consist of a large number of components each with a relatively small failure probability. For prognostic purposes there are quite few of the failure mechanisms that can be identified using measured data [3]. An approach to categorize the different failures and their failure precursors is to divide electrical systems into six different prognostic levels, as proposed in [1]. These levels are listed in Table I.

A. Failure sources for the on-chip level and components

In the on-chip level (level 0) there are mainly three categories of failure mechanisms present: Hot-carrier injection damage, Dielectric breakdown, and Electromigration [13]. Hot carrier damage has been identified as the major cause for aging in deep submicron processes [6], [7] and will be the focus of section IV.

Gate-oxide failure results from time-dependent dielectric breakdown (TDDB). In this case the dielectric fails when a conductive path is formed through the gate to either source or drain in a CMOS transistor. This effect will be present for aging devices even if they are operated under normal voltage conditions. Increase in electric fields for the devices will accelerate the TDDB process [13]. Moreover, in modern CMOS processes with extremely thin gate oxides the aging process is likely to get worse. However the TDDB process in modern CMOS is not very well understood [13]. Furthermore, dielectric breakdown is also present on discrete semiconductor components (level 1), such as diodes and capacitors.

TABLE I. PROGNOSTIC LEVELS

Level	Description
Level 0	Chip and on-chip devices
Level 1	Discrete components and encapsulated chips
Level 2	Printed circuit board and the interconnect between components
Level 3	Enclosure, chassis and connections for circuit boards
Level 4	Entire electronic system
Level 5	Multi-electronic systems and their interconnect

Electromigration is a result of increased current densities on interconnects and contacts on-chip. Higher integration and shrinking feature sizes at the same time as power-supply voltages are relatively constant has made electromigration a concern for reliability. Formation of metal voids on interconnects will cause open circuits or high resistive paths, which in turn can result in poor performance or circuit malfunction [13]. Furthermore, electromigration can also form metal voids in connection to contacts between metals and the silicon. When the metal void grows the aluminum can diffuse down to the silicon. This in turn can cause metal spikes to form deep in the silicon region, thus shorting the p-n junctions [14].

B. *Failure sources for circuit boards*

Components in package and the printed circuit board, which comprise level 1 and 2, have similar failure mechanisms. The main failure mechanisms on theses levels are environmental fatigue of different sorts (i.e. vibration, temperature, etc.) and corrosion. Temperature effects include cycle fatigue in soldering joints and chip-to-board bond-wires due to large variations in operation temperatures. This results in open circuits for bonds and solder-joints. Both temperature cycling and vibration are common effects in airplane systems, making broken solder-joints a likely cause of failure [15], [16].

C. *Failure sources for large electronic systems*

The two dominating failure mechanisms for level 3 to level 5 are mechanical wear-out and corrosion. Each of these mechanisms manifests themselves as open circuits for the connections between the different circuit boards, cards, and systems. Both corrosion and mechanical wear-out seem to be likely to occur for avionic systems.

IV. MECHANISMS OF FAILURE

Trends in the power supply current variations depend on how the circuit and devices degrade from aging. In order to simulate the effect of aging the basic modeling of the degradation is based on the physics behind the Hot Carrier Injection (HCI) phenomena [6], [7].

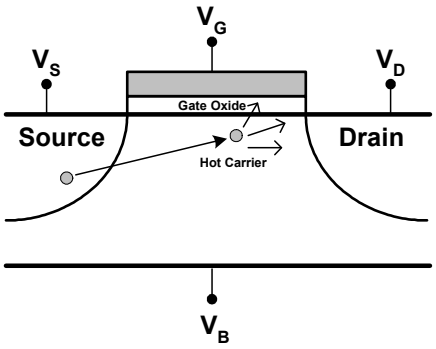

Figure 2. Hot carrier injection phenomenon in MOSFET transistors.

In semiconductor devices when an electron or a hole gains very high kinetic energy after being accelerated by a strong electric field it becomes a hot carrier or hot electron. Since hot carriers have a high kinetic energy, they can be injected and trapped in a different area of the device as shown in Fig. 2. This phenomenon is called *hot carrier injection*. In MOSFET technology, as the devices begin to age, because of the hot carrier injection phenomenon the gate dielectric is degraded. The leakage current gradually increases and the threshold voltage of the device is shifted. Ultimately this phenomenon can bring the device in an unstable condition in which the device fails in its normal operation.

Based on [17], some hot carrier injection mechanisms are: 1) Drain avalanche hot carrier injection, where channel carriers are accelerated into the drain's depletion region. 2) Channel hot electron injection, where electron-hole pairs formed in the collision with silicon lattice atoms can overcome the potential barrier and get trapped in the oxide. 3) Substrate hot electron injection, where carriers, due to a large bulk bias condition, migrate towards the gate oxide and can get trapped there. When the number of hot carriers trapped in the interface between doped regions grows over time a volume charge is formed. Due to this reason the threshold voltage, V_{th}, and conductance, g_m, of the device are changed as the device begins to age.

In order to simulate aged circuit behavior the aging is assumed to be dominated by HCI degradation and the resulting gate-oxide degradation [6], [7]. To perform an analysis of the degradation effect on power supply current trends the degradation is parameterized by the variable Δ, which denotes the relative increase/decrease of the circuit parameters V_{th}, g_m and the saturation current, I_{dsat}, of the NMOS and PMOS transistors. This model is compliant with the HCI degradation in [17] and the gate-oxide degradation that is investigated in [18].

V. ANALYSIS OF THE POWER SUPPLY CURRENT OF A CIRCUIT

With the background of primary sources for on-chip aging we now give an introduction to how the power supply current can be used to gain information about the circuit health. This information could later be used in the estimation of current health and therefore the remaining useful life-time. The analysis of power supply current is not new and it is used for static measurements in product testing and dynamic measurements to acquire coded data in security applications.

A. I_{DDQ} Testing

Static analysis of the power supply current is already well established methodology within the semiconductor industry. It is commonly used for product testing of CMOS integrated circuits through the I_{DDQ} test method. The current drawn from the power supply, I_{DD}, is measured in the quiescent (steady) state. In a CMOS circuit, the quiescent supply current is relatively low, ideally only consisting of leakage current but in the presence of defects, such as bridging, shorts, etc. the supply current can be higher than expected as shown in Fig. 3. The information provided by I_{DDQ} testing helps to gain insight about the health condition of the CMOS integrated circuits [19]. However this test method is only suited for detecting the defects in a faulty system.

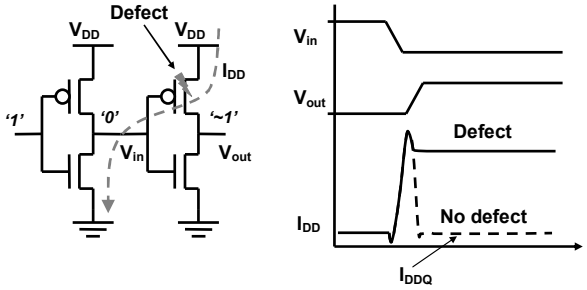

Figure 3. Principle of I_{DDQ} testing.

B. DPA Attacks

The concept of using dynamic measurements of the power supply current during run-time as a source of information about internal states is also an established method. It has received much attention the last years in the context of security as a mean for retrieving encrypted data from secure devices. The Differential Power Analysis Attack (DPA) described in [20], [21] is a powerful tool used for this purpose. The attack works because the instantaneous power supply current of a circuit depends on the internal states. From the known output and supply current specific information such as encryption keys can be extracted by using the statistical information available in a large number of supply current measurements.

C. Power Analysis for Circuit Aging

The methods used in this paper combine existing ideas to gain information about the current health of an electronic system based on the measurements of the power supply current. The assumption, which will later be verified by circuit simulations, is that circuits that degrade primarily from HCI will experience a shift in the spectral density of the supply current towards lower frequencies. By comparing how the statistical properties of the samples vary compared to a fresh circuit the health and remaining useful life-time can be estimated by mapping against a reference aging curve.

Two reference designs are studied and are chosen as being representative for system-on-chip (SoC) circuits. First a ring oscillator is considered which is a traditional circuit used for the investigation of circuit aging. The second reference systems is a 15-to-4 bit adder corresponding to a digital processing unit.

As the power supply is only measurable at the chip boundaries, the degradation of individual subsystems will affect the total power dissipation measurements of the chip. By showing that the analysis works on the power supply of individual sub-systems as well as for complex systems, we can consider the entire chip as a black box and the measurement point can be accessed off-chip. This means that no modifications of existing systems needs to be made, maintaining the system performance and without compromising safety.

D. Reference Systems

The circuit we chose to represent a basic general system is a 5-stage ring oscillator as shown in Fig. 4. Ring oscillators are used for on-chip clock generation and their functionality is often studied when investigating the aging effect on the device (transistor) level. The output of the ring oscillator is a square wave with a frequency that is dependant of the delay through the inverters. When the circuit ages the rising and falling

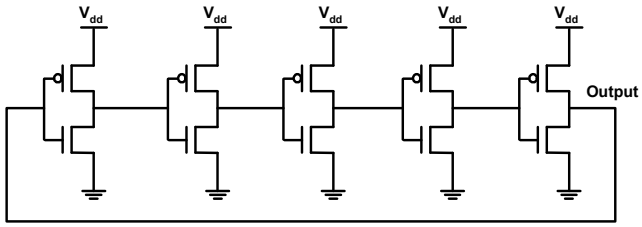

Figure 4. A 5-stage ring oscillator reference system.

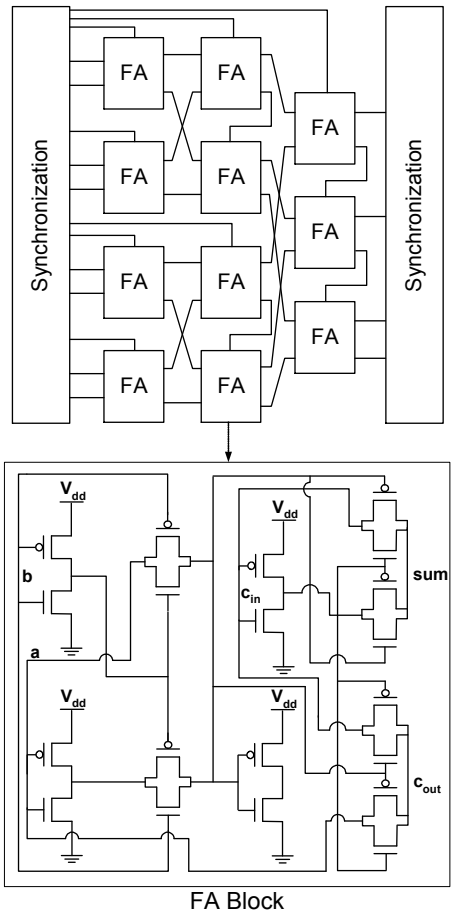

Figure 5. A 15-to-4 bit adder reference system.

delays of the inverter will change resulting in a shift in the oscillation frequency.

The 15-to-4 bit adder, seen in Fig. 5, is chosen to represent a general digital sub-system. The functionality is such that the 15 1-bit input signals are added to get a 4 bit binary representation. Such digital building blocks are for example a part of Flash ADC Decoders, Multipliers, and Carry Save Adders. The actual design consists of 11 Transmission gate Full Adders that were chosen for a low power-performance trade-off.

E. Simulations

The circuit simulations are performed using Cadence Spectre circuit simulator in a 90-nm CMOS process. An example on how the degradation affects the time domain performance of the digital reference system is shown in Fig. 6. It can be seen that the circuit reacts slower to a change in the input conditions, causing a delay and a reduction in the supply current peak. This is compliant with our earlier assumption that the energy will be shifted towards lower frequencies. It can be observed by a reduction in the power weighted mean frequency by 10% of the circuit clock frequency, which also reduces the variance in the supply current samples.

VI. Power Analysis for Prognostics

As the circuit degrades over time the estimation of the current system health, $F(t)$, will decrease and a threshold J can be defined such that the circuit performance is unacceptable if $F(t) < J$. The RUL at time t_0 is then given by $t - t_0$ where t is an approximation of the solution to the equation $F(t) = J$.

A widely accepted empirical relationship between the parameter deviation $\Delta(t)$ and the elapsed stress time can be used to write $F(t)$ as a function of the stress time t. The relationship for the HCI degradation mechanism is [22], [23]:

$$\Delta(t) = kt^{\alpha} \tag{1}$$

where k and α are two parameters. This model has been verified under static or periodically repeated AC stress. The parameter α depends little on operating stress while k depends heavily on the operating conditions such as the drain current and channel electric field. In Sections VI.A-C the mean and variance of the supply current measurements will be used for health estimators $F(t)$ and it will be shown that $F(t)$ is approximately an affine function of Δ. By combining such approximation with (1), the system health estimation can be written as a function of the elapsed stress time

$$F(t) = F(0) - ct^{\alpha} \tag{2}$$

where c is an operating stress dependent parameter and α a known circuit dependent constant. By using this relation and following the approach described in [23], a maximal likelihood estimate of the remaining useful life can be obtained under some natural statistical conditions.

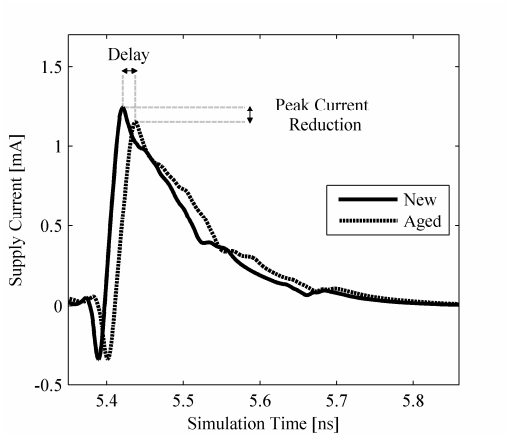

Figure 6. Simulation of the supply current under one clock cycle for the digital reference system.

A. Mean power supply current for health estimation

The first estimation of the system health $F_1(t)$ will be based on the mean power supply current variations. We first assume that each time a health estimation should be performed a given input sequence is applied and the mean power supply current is measured. This method is applied to the oscillator, adder and a system consisting of both together. Fig. 7 shows the simulated mean power supply current for a test cycle as a function of the level of degradation Δ. In the simulations, the adder produced faulty outputs for degradation parameters larger than 0.13 due to timing violations. The simulations show that the health estimation through the mean power supply current of the circuit, $F_1(t)$ is a monotonously decreasing function of the level of degradation Δ and can be approximated with an affine function as in (2).

B. Power supply current variance for health estimation

The second estimation for the system health $F_2(t)$ is more general and is based on the variance of the power supply current measurements. It follows from the earlier assumption that the spectral density of the power supply current will be shifted towards the lower frequencies when the circuit degrades, reducing the variance. The simulation of the systems is shown in Fig. 8. As the $F_2(t)$ also is a monotonously decreasing function the same RUL estimations as earlier can be applied.

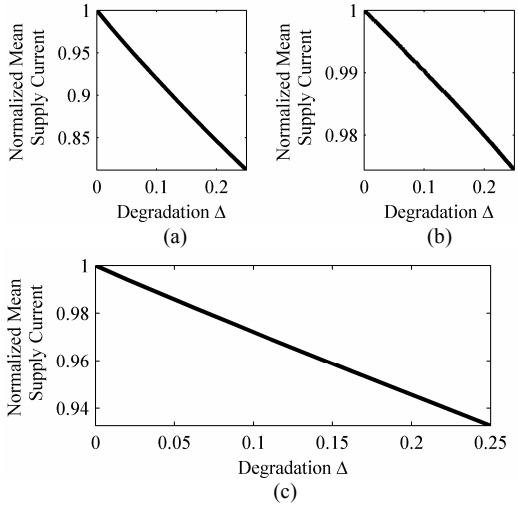

Figure 7. Normalized mean power supply current for the two individual reference systems (a) - oscillator, (b) - adder and the two systems together (c).

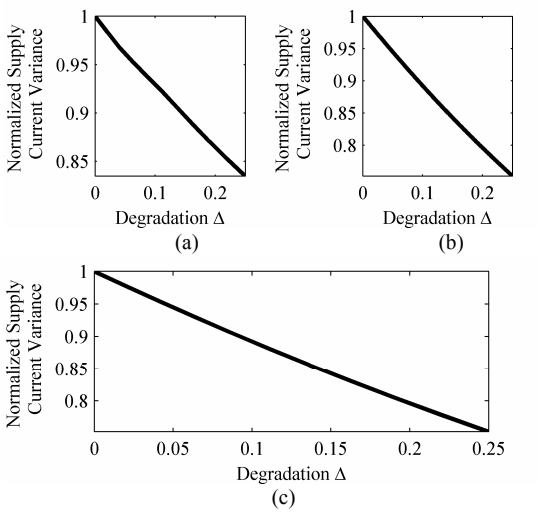

Figure 8. Normalized power supply current variance for the two individual reference systems (a) – oscillator, (b) - adder and the two systems together (c).

The definition of what is a faulty circuit depends on the application, for a performance critical system a functional error is likely to occur before a hard error in a device while a system with less demanding performance requirements might suffer failures such as shorts, opens or hard oxide breakdowns. Independent of our definition of a faulty device we can define a health threshold, *J*, such that the above methods are applicable.

C. *Supply current measurements with unknown inputs*

In the previously described approach, normal operation of the circuit has to be interrupted such that prognostics can be performed by analyzing the supply current of the circuit when a specific test input is applied. However, it is possible to do prognostics using supply current measurements during normal operation if the activity is fairly constant over time.

Instead of using a test sequence, a random sequence has been applied to the adder. Let X_i^j be a random variable describing the supply current of transistor i at clock cycle j. The random variables X_i^j for different i and j are assumed to be independent and identically distributed. From the central limit theorem, it follows that the sum:

$$S_j = \sum_{i=1}^{n} X_i^j \qquad (3)$$

converges towards a normal distribution when n tends to infinity.

For the adder circuit, Fig. 9 and 10 show that the mean supply current for clock cycles are approximately identically and normally distributed. By averaging the mean supply current over N clock cycles, the standard deviation can be reduced by a factor $N^{0.5}$ and sufficient accuracy can be obtained. This is comparable to the technique used in DPA attacks where power supply differences caused by a '0' or '1' at a single node or bus-wire can be detected. Fig. 11 shows the result of averaging over N =1000 clock cycles for each level of degradation. Since the mean is taken over a large number of clock cycles, the supply current of different gates do not need

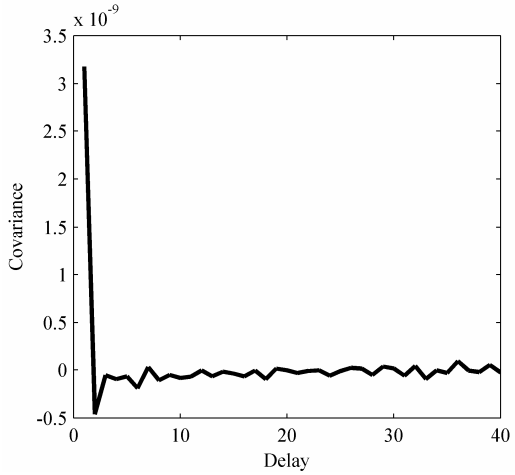

Figure 9. Covariance function estimate for the mean current in each cycle. If the data is independent the covariance function is a Dirac function.

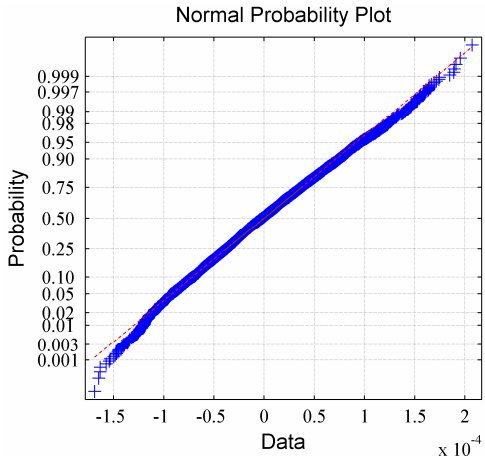

Figure 10. A normality plot of the mean current of each cycle. If the data are normal distributed the plot will be linear.

to be identically distributed, it is sufficient that the supply current in different clock cycles are identically distributed for each of the gates. This means that this approach could be applied in more general situations. In conclusion, the trend of the mean supply current can be used for RUL estimations during normal operation of the circuit.

VII. Applications and Discussion

The ability to perform prognostics of electronic systems using the power supply current is based on the nature of the power supply current of CMOS devices. This has a dependence on the internal states which is common for general circuits, something which is also utilized for I_{DDQ} testing.

A complex system will have a power supply current that is a superposition of supply current from all sub-systems. This will have several implications: first, the ability to apply the prognostic methods to complex systems is possible, which is necessary as entire systems are implemented on a single chip. For example, traditional external analog systems as DC-DC converters are merged with digital systems in current system-on-chip architectures. Secondly the measurement of the supply

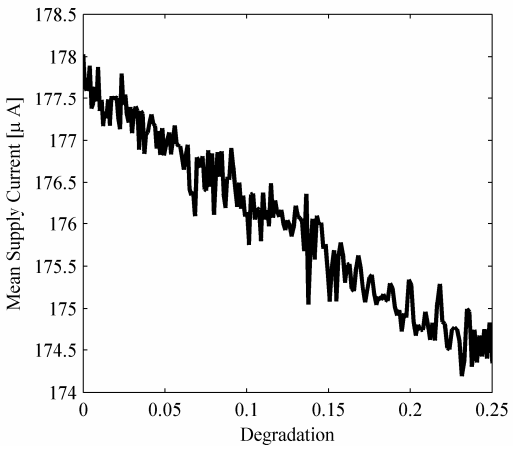

Figure 11. The plot shows the simulated mean supply current over 1000 clock cycles for each degree of degradation.

current does not have to be done at the device level. The power measurements can be conducted at the chip boundary, the circuit board connection point or even higher up in the prognostic levels making the method very promising.

If now other failure sources, such as corrosion or damaged solder joints, also degrade the electrical properties through for example increased resistance, their degradation would also affect the supply current. By applying this prognostic method at a higher prognostic level we have the potential of detecting all errors caused at lower levels without actually performing the measurement at those specific levels. If the degradation of different sources vary depending on the operation, measurements could be required at several points to identify the critical source. As the method does not require the alteration of components or devices it becomes a suitable method for introducing prognostics at the system level when the components used can be purchased from vendors.

VIII. CONCLUSION

Prognostics of electronic systems exhibit great potential in increasing the safety, reliability and availability of avionic systems. However, the prognostic concepts in the context of avionics have mostly been developed for mechanical systems.

As electronic systems can consist of both Application Specific Integrated Circuits (ASICs) with full knowledge of the design and COTS components without design knowledge, a prognostic method for electronic systems must be able to deal with general system-on-chip components.

This paper has presented an introduction to such a prognostic method for electronic systems based on power supply current trends that is applicable on-chip, on circuit board or higher prognostic levels. According to the presented simulation results and discussion, there is a measurable relationship between aging and power supply current variations with time. This relationship can be utilized as a prognostic method for electronics-dependent systems at any prognostic level.

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